

Module No.	Unit No.	Topics	Hrs.
<b>1.0</b>		<b>Review of MOSFET operation and Fabrication</b>	<b>08</b>
	<b>1.1</b>	Overview of VLSI Design Flow, Review of MOSFET operation, MOSFET Capacitances, MOSFET scaling, Short channel effects	03
	<b>1.2</b>	Fabrication process flow of NMOS and CMOS, Lambda based design rules	03
	<b>1.3</b>	Novel MOSFET Architectures FinFET, GAA-FET, CNTFET	02
<b>2.0</b>		<b>Combinational CMOS Logic Circuits</b>	<b>06</b>
	<b>2.1</b>	CMOS inverter operation, Voltage Transfer characteristics (VTC), Noise Margins, Propagation Delay, Power Dissipation, Design of CMOS Inverter, Layout of CMOS Inverter	03
	<b>2.2</b>	Realization of CMOS NAND gate, NOR gate, Complex CMOS Logic Circuits, Layout of CMOS NAND, NOR and complex CMOS circuits	03
<b>3.0</b>		<b>MOS Design Logic Styles</b>	<b>09</b>
	<b>3.1</b>	Static CMOS, Pass Transistor Logic, Transmission Gate, Pseudo NMOS, Dynamic Logic, Domino Logic, NORA, Zipper, C <sup>2</sup> MOS	04
	<b>3.2</b>	Setup time, Hold time, clocked CMOS SR Latch, CMOS JK Latch, MS –JK Flip Flop, Edge triggered D-Flip Flop and realization using design styles	03
	<b>3.3</b>	Realization of Shift Register, MUX, Decoder using above design styles ,1-bit full adder	02
<b>4.0</b>		<b>Semiconductor Memories</b>	<b>06</b>
	<b>4.1</b>	ROM array, 6T-SRAM (operation, design strategy, leakage currents, sense amplifier), layout of SRAM	03
	<b>4.2</b>	Operation of 1T and 3T DRAM Cell, NAND and NOR flash memory	03
<b>5.0</b>		<b>Data path and system design issues</b>	<b>06</b>
	<b>5.1</b>	Ripple carry adder, CLA adder, carry save adder, carry select adder, carry skip adder, Array Multiplier	04
	<b>5.2</b>	On chip clock generation and distribution, Interconnect delay model, interconnect scaling and crosstalk	02
<b>6.0</b>		<b>RTL Design</b>	<b>04</b>
	<b>6.1</b>	High Level state machines, RTL design process	02
	<b>6.2</b>	RTL design of Soda dispenser machine, FIR Filter	02
<b>Total</b>			<b>39</b>